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BRIEF

Getting the most out of your instrumentation amplifier design

By Thomas Kugelstadt • Senior Systems Engineer, Industrial Systems

Introduction

Many industrial and medical applications use instrumentation amplifiers (INAs) to condition small signals in the presence of large common-mode voltages and DC potentials. Standard INAs using a unity-gain difference amplifier in the output stage, however, can limit the input commonmode range significantly. Thus, commonmode signals induced by adjacent equipment, as well as large differential DC potentials from differently located signal sources, can increase the input voltage of the INA, causing its input stage to saturate. Saturation causes the INA output voltage, although of wrong value, to appear normal to the following processing circuitry. This could lead to disastrous effects with unpredictable consequences.

This article reviews some principles of the classic three-op-amp INA and provides design hints that extend the input commonmode range to avoid saturation while preserving overall gain at maximum value. The article also discusses the removal of large differential DC voltages through active filtering, avoiding passive RC filters at the INA input that otherwise would lower its common-mode rejection ratio (CMRR).

INA principles

Figure 1 shows the block diagram of the classic three-opamp INA. The inputs, V_{IN+} and V_{IN-}, are defined through the input polarities of the difference amplifier, A3.

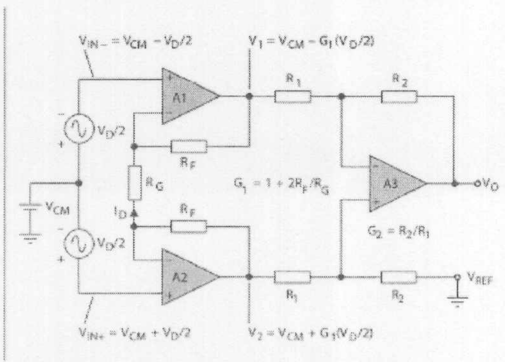

Figure 1. Classic three-op-amp INA and its voltage nodes

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By definition, the INA's input signals are subdivided into a common-mode voltage, V_{CM}, and a differential voltage, V_D. While V_{CM}, the voltage common to both inputs, is defined as the average of the sum of V_{IN+} and V_{IN-}, V_D represents the net difference between the two.

$$(1)\quad V_{CM} = \frac{V_{IN+} + V_{IN-}}{2} \text{ and } V_D = V_{IN+} - V_{IN-}.$$

Solving both equations for V_{IN+} or V_{IN-} and equating the received terms results in a new set of equations, which, when solved for either input voltage, yields

$$(2)\quad V_{IN+} = V_{CM} + \frac{V_D}{2} \text{ and } V_{IN-} = V_{CM} - \frac{V_D}{2}.$$

In the nonsaturated mode, the op amp action of A1 and A2 applies the differential voltage V_D across the gain resistor, R_G, generating the input current, I_D:

$$(3)\quad I_D = \frac{V_{IN+} + V_{IN-}}{R_G} = \frac{V_D}{R_G}.$$

The output voltages of A1 and A2 are therefore

$$V_1 = V_{CM} - \frac{V_D}{2} - I_D R_F \text{ and } V_2 = V_{CM} + \frac{V_D}{2} + I_D R_F.$$

Replacing current I_D with Equation 3 yields

$$(4)\quad V_1 = V_{CM} - \frac{V_D}{2} G_1 \text{ and } V_2 = V_{CM} + \frac{V_D}{2} G_1,$$

where $G_1 = 1 + 2\frac{R_F}{R_G}$.

Equation 4 shows that only the differential component, $V_D/2$, is amplified by the input gain, G_1, while the commonmode voltage, V_{CM}, passes the input stage with unity gain. The difference amplifier, A3, subtracts V_1 from V_2 and amplifies the difference with the gain G_2:

(5) $$V_O = (V_2 - V_1)G_2, \text{ where } G_2 = \frac{R_2}{R_1}.$$

Inserting Equation 4 into Equation 5 and solving for V_O/V_D provides the transfer function of the INA:

(6) $$\frac{V_O}{V_D} = G_1 G_2 = G_{TOT}.$$

Extending the input common-mode voltage range

Note that V_1 and V_2 in Equation 4 do not represent absolute voltages. Because V_{CM} and V_D can change their polarities, the maximum voltage either output can assume before reaching saturation is

$$\pm\left|V_{1,2}\right| = \pm\left(\left|V_{CM}\right| + \left|\frac{V_D}{2}\right|\right) \le \pm\left|V_{SAT}\right|.$$

For clarification, the following description simply ignores signal polarities, and the variables refer only to magnitude values. Assuming that $V_{1,2}$ and $V_D/2$ are constant, the only way to increase the input common-mode voltage from V_{CM} to V_{CM}' is to reduce the input gain from G_1 to G_1' so that

$$V_{1,2} = \text{constant} = V_{CM} + \frac{V_D}{2}G_1 = V_{CM}' + \frac{V_D}{2}G_1'.$$

Solving for V_{CM}' yields

$$V_{CM}' = V_{CM} + \frac{V_D}{2}\left(G_1 - G_1'\right).$$

Reducing G_1 reduces the range of the amplified differential component, G_1' ($V_D/2$), thus providing an expansion range for V_{CM}. Standard INAs, using unity-gain difference amplifiers, have $R_2 = R_1$ and $G_2 = 1$.

The total INA gain is then placed into the input stage, making $G_1 = G_{TOT}$. Equation 6 shows that reducing G_1 from G_{TOT} to G_1', while preserving G_{TOT}, requires an increase in difference amplifier gain from $G_2 = 1$ to $G_2' = G_{TOT}/G_1'$.

(7) $$V_{CM}' = V_{CM} + \frac{V_D}{2}G_{TOT}\left(1 - \frac{1}{G_2'}\right)$$
$$= V_{CM} + \frac{V_D}{2}G_1'\left(G_2' - 1\right).$$

Replacing G_1 with G_{TOT} and G_1' with G_{TOT}/G_2' results in the extended common-mode range:

This improved common-mode range at the amplifier output is now passed on 1:1 to the input. Applying gain to the difference amplifier requires access to the feedback resistor of A3 in Figure 2. A common solution uses a stand-alone difference amplifier, which provides access to the feedback resistor via a V_{SENSE} pin. The input stage is then realized by a dual low-noise amplifier, with external resistors R_F and R_G being used to set the input gain.

To raise the gain of a unity-gain amplifier, external resistors can be switched in series to R_2. However, the internal resistor values must be measured, as they can deviate by ±30% from their nominal values given in the datasheet. This approach works well for moderate gain. For large gain, however, the external resistors can reach prohibitive values, increasing noise to an undesirable level. A buffered voltage divider in the feedback path of A3 is then required.

Resistors R_3 and R_4 allow a wide range of gain settings with moderate resistor values. Voltage follower A4 provides low output impedance, which preserves the high CMRR of the difference amplifier.

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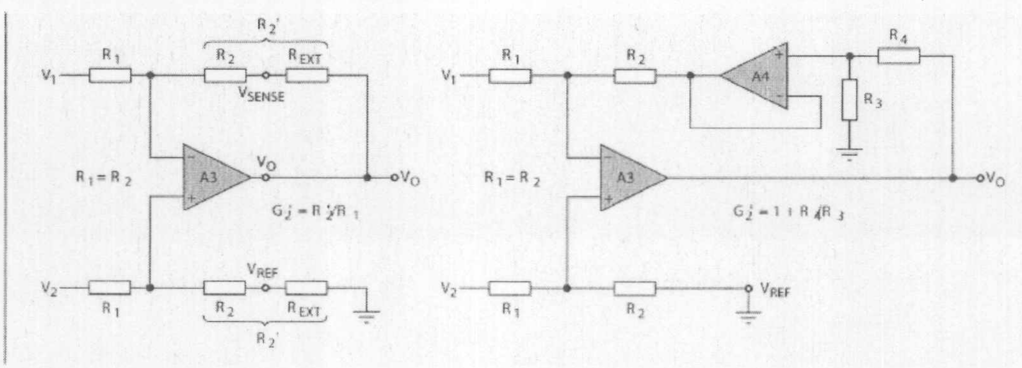

Figure 2. Increasing difference amplifier gain via REXT or buffered voltage divider

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The circuit in **Figure 1** incorporates two force-balance nulling techniques. To follow the operation, assume that all the switches are open and then close S_2 and S_3, thereby engaging ultraprecision integrating amplifier A_2 and forcing A_1's output to ground. A_1's input offset appears at its positive input, and C_1 stores 101 times this offset. Opening S_3 allows A_1 to function normally again, but with 1 mV of effective offset and approximately 1 mV/sec of drift. Now, opening S_2 puts feedback resistor R_1 in the circuit and causes an output voltage equal to $I_{BIAS} \times R_1$—typically, 1 mV. Closing S_4 and S_5 nulls A_1's output again, but this time through A_3. A_1's bias current now goes through R_2, and C_2 stores it as a voltage at 60 mV/pA. Opening S_4 ends the nulling phase.

Closing S_1 connects the input drive—the resistor under test—and a voltage source. Although the amplifier is now nearly perfect, it doesn't remain so for long. Drift on capacitors C_1 and C_2 requires a new nulling phase within several seconds; otherwise, the amplifier's specifications may degrade beyond those of an unaided LTC6241. **Figure 2** shows a simpler method. Rather than trying to perfect the amplifier, this circuit instead chops the excitation to allow subtraction of the amplifier contributions. Also, the resistor under test is now in the feedback path, so the output is proportional to the resistor's resistance rather than its admittance. Rise time is 10 msec (10 to 90%) with a 1-GΩ resistor, so the excitation should be no faster than about 10 Hz to ensure adequate settling.

PROTECTING A HIGH-IMPEDANCE CIRCUIT

How can you protect a high-Z circuit without affecting its input impedance? Strictly speaking, you can't, but you can come close. One of the best ways is to use a series resistor and some series inductance, even if it's just a length of trace. The inductance and parasitic elements spread out an ESD (electrostatic-discharge) pulse and improve the odds that it will jump to a chassis before it gets to anything sensitive. You can further improve those odds by introducing a spark gap in the layout near the connector pin to be struck. This approach is cheap and effective, but it can cause problems in higher density digital designs. The spark gap re-emits a strong EMI (electromagnetic-interference) wave, including some eerie blue. This phenomenon repeatedly crashed an onboard but distant 486 microprocessor, fortunately without harming the hardware. The protection you require depends on the level of immunity you specify for the design. In this case, the spark gap is a failure, because designers did not allow for PC-reset interventions. For analog designs or simple digital designs, spark gaps should not be a problem. Gas-discharge tubes, which are also available as components, are other alternatives.

Almost anything you do with diode clamps can cause leakage. Schottky diodes are probably out of the question because they tend to leak more. Ultralow-leakage diodes include the CMPD6001 series from Central Semiconductor (www.centralsemi.com) and the BAS416 from Philips. But the maximum-leakage specification, even when devices are cold, is 500 pA to 5 nA. The high-temperature specifications are even worse, often running into microamps. For the lowest leakage performance, JFET junctions still outperform diodes. The 2N4393, available from Vishay in an SOT-23 package, typically leaks 5 pA at room

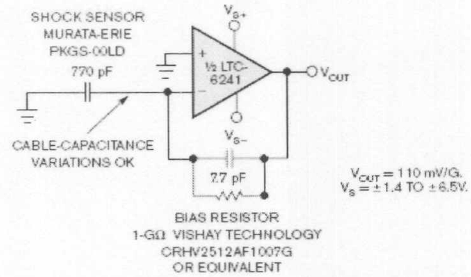

Figure 4 In this classic inverting-charge amplifier, variations in cable capacitance–that is, length–do not affect the signal gain. Use this circuit when the accelerometer is remote from the amplifier and the cable length is unspecified. Drawbacks are that the low-valued feedback capacitor sets the gain, and the bias resistor working into the same feedback capacitor determines the low-frequency performance.

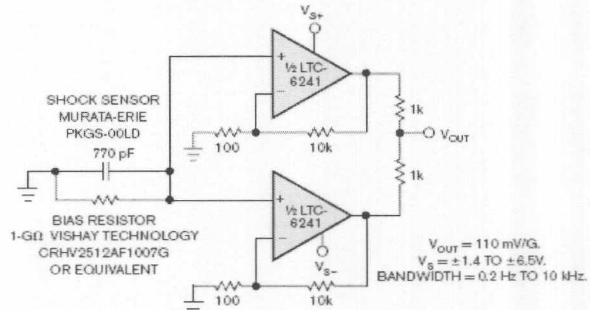

Figure 5 This noninverting-charge amplifier offers two advantages: You can connect stages in parallel to reduce voltage noise, and the bias resistor works into higher capacitance for better low-frequency response.

temperature and 3 nA at 100°C (**Figure 3**). Compare this leakage with the maximum-specified bias current of 75 pA at 70°C for the LTC6241. Adding even good diodes can cause a significant degradation. Some design work can help offset this problem, however. For example, consider the tracking-limiter circuit (**Figure 3**). A_2 back-biases the diodes, and C_1 stores the average dc voltage. The system shunts overvoltages and spikes to the reservoir capacitor but allows dc through with unity gain, protecting the inputs and improving input-overload-recovery time. For dc gain, simply short C_1 and move the input from A_2 to A_1's inverting input; inverting circuits are easier to protect, because you can simply connect the diodes to ground.

HOW HIGHER Z HELPS

Figures 4 and **5** show two approaches to amplifying signals from a capacitive sensor. The sensor in both cases is a 770-pF piezoelectric shock-sensor accelerometer, which generates charge under physical acceleration. **Figure 4** shows the classic charge-amplifier approach. The op amp is in the inverting configuration, so the sensor looks into a virtual ground. The op-amp action forces all of the charge the sensor generates

across the feedback capacitor. Because the feedback capacitance is 0.01 times the sensor capacitance, the voltage across the feedback capacitor is 100 times what would have been the sensor's open-circuit voltage. So, the circuit gain is 100. The benefit of this approach is that the circuit's signal gain is independent of any cable capacitance between the sensor and the amplifier. Hence, designers favor this circuit for remote accelerometers whose cable length may vary. Difficulties with the circuit are inaccuracy of the gain setting with the small capacitor and low-frequency cutoff because the bias resistor works into the small feedback capacitor.

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Figure 5 shows a noninverting-amplifier approach. This approach has many advantages. First, resistors, rather than a small capacitor, accurately set the gain. Second, the low-frequency response improves because the bias resistor working into the large 770-pF sensor, rather than into a small feedback capacitor, dictates the cutoff frequency. Third, you can sum and make parallel the noninverting topology for scalable reductions in voltage noise. This circuit's only drawback is that the parasitic capacitance at the input slightly reduces the gain. This circuit is a good fit for applications in which parasitic input capacitances, such as traces and cables, are relatively small and invariant.

When you calculate the bias resistance for the desired low-frequency cutoff, consider that you may want to make the bias resistor's value still larger. Doing so reduces the noise floor at low frequencies. For example, if you want to support frequencies as low as 10 Hz at -3 dB, the bias resistor works out to $1/2\pi\times10\ \text{Hz}\times770\ \text{pF}=20\ \text{M}\Omega$. At 10 Hz, the 20-M$\Omega$ resistor contributes 580 nV/$\sqrt{\text{Hz}}$ of noise, which is 3 dB down, just like the signal. If you make the resistor value 1 GΩ, the accelerometer capacitance effectively attenuates the resistor's 4000-nV/$\sqrt{\text{Hz}}$ noise to 80 nV/$\sqrt{\text{Hz}}$, but the signal is barely attenuated. Sometimes, impedance higher than that normally required actually helps.

Devices and materials are available to support and protect high impedances. Dealing with high impedance requires a knowledge of what are otherwise minuscule phenomena. Sometimes, quantization of phenomena such as current noise can be challenging, but with the right circuit techniques, measurements become meaningful and repeatable. A proper breakdown of error sources, such as leakage, settling time, voltage noise, and current noise, helps the circuit designer to know what to expect. EDN

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AUTHOR'S BIOGRAPHY

Glen Brisebois is an applications engineer responsible for customer support for op amps, comparators, references, and rms-to-dc converters at Linear Technology Corp (Milpitas, CA). He holds bachelor's degrees in physics and electrical engineering from the University of Alberta (Edmonton, AB, Canada).